

LISTING OF CLAIMS:

1. (Original) A fast Fourier transform (FFT) circuit in which butterfly modules may be selectively pruned for use in specific applications, the circuit comprising:

a plurality of computational stages connected in sequence, each computational stage comprising a plurality of butterfly modules connected between multiple input lines and multiple output lines, wherein the computational stages and the butterfly modules are connected to perform an FFT operation on a plurality of input signals applied to a first of the computational stages;

and wherein each of the butterfly modules comprises means for forcing each of its outputs selectively to zero, whereby a zero output from a butterfly module affects at least one module downstream of the zero output and minimizes power dissipation in the at least one affected module.

2. (Original) A fast Fourier transform (FFT) circuit as defined in claim 1, wherein the means for forcing outputs selectively to zero comprises a multiplexer for each output of a butterfly module, the multiplexer having:

a first input, to which the output of the butterfly module is connected;

a second input connected to a zero signal;

a control line for selecting between the two inputs; and

an output for coupling the selected input to a subsequent computational stage;

and wherein components connected downstream of a zero output signal are effectively pruned from the circuit.

3. (Original) A fast Fourier transform (FFT) circuit as defined in claim 2, wherein:
selected butterfly modules in one of the computational stages are effectively pruned by forcing
selected outputs of prior butterfly stages to zero.

4. (Original) A method for effectively pruning a fast Fourier transform (FFT) circuit
having a plurality of successive computational stages, each of which includes a plurality of
butterfly modules, the method comprising:

determining which butterfly modules need to be pruned for a particular application of the
FFT circuit; and

forcing the input signals of the butterfly modules located in the determining step to zero,
whereby the selected butterfly modules are effectively pruned from the circuit because of their
zero inputs.

5. (Currently Amended) A method for effectively pruning a fast Fourier transform (FFT)
circuit having a plurality of computational stages, each of which includes a plurality of butterfly
modules, the method comprising:

determining which butterfly modules need to be pruned for a particular application of the
FFT circuit; and

forcing the input signals of the butterfly modules located in the determining step to zero,
whereby the selected butterfly modules are effectively pruned from the circuit because of their
zero inputs.

~~A method as defined in claim 4 wherein:~~

wherein the step of forcing the input signals to zero is effected by forcing the corresponding output signals in a prior computational stage to zero.

6. (Currently Amended) A method for effectively pruning a fast Fourier transform (FFT) circuit having a plurality of computational stages, each of which includes a plurality of butterfly modules, the method comprising:

determining which butterfly modules need to be pruned for a particular application of the FFT circuit; and

forcing the input signals of the butterfly modules located in the determining step to zero, whereby the selected butterfly modules are effectively pruned from the circuit because of their zero inputs,

~~A method as defined in claim 4, wherein:~~

wherein the step of forcing the input signals to zero comprises using a multiplexer to inject a zero signal into a controlled signal line.

7. (Original) A method as defined in claim 6, wherein:

the step of using a multiplexer comprises applying a prune control signal unique to each controlled signal line, to select a zero signal.

8. (New) A method of pruning a fast Fourier transform (FFT) circuit, the FFT circuit includes an initial computational stage and one or more successive computational stages, each of the initial computational stage and the one or more successive computational stages includes a plurality of butterfly modules, the method comprising:

determining if one or more butterfly modules of the one or more successive computational stages need to be pruned for a particular application of the FFT circuit; and

forcing the input signals of the one or more butterfly modules determined as needing to be pruned to zero to thereby effectively prune the one or more butterfly modules.